DESIGN OF HIGH SPEED AND LOW POWER SENSE AMPLIFIER FOR SRAM APPLICATIONS

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Abstract: A high performance sense amplifier (SA) circuit for low power SRAM applications is presented in this work. My focus will be to improve the power consumption and response time of this sense amplifier. The transistor stage number of the proposed SA from V_{DD} to GND is reduced for fast low voltage operation. Thus the proposed sense amplifier which is implemented in 0.18um CMOS process can work at 100MHz with voltage as low as 1.5V.Power consumption and delay have trade off,so we have to optimized the parameters according to our requirement.A great investigation is done in this thesis for power consumption and delay time. I observed the variation in these two parameters by varying the operating frequency,load and sizing of tail transistor of sense amplifier.

Keyword: Bitlines ,CMOS, Delay,Power Consumption, Precharge, SRAM,Sense Amplifier.

1 INTRODUCTION

One of the major issues in the design of SRAMs is the memory access time (or speed of read operation). For having high performance SRAMs, it is essential to take care of the read speed both in the cell-level design and in the design of a clever sense amplifier. Sense amplifiers are one of the most critical circuits in the organization of CMOS memories. Their performance strongly influences both memory access time and overall memory power consumption. High density memories commonly come with increased bit line parasitic capacitances. These large capacitances slow down voltage sensing and makes bit line voltage swings energy-consuming, which result in slower more power hungry memories. Need for larger memory capacity, higher speed, and lower power dissipation imposes following trade offs in the design of sense amplifier:

1) Increase in number of cells per bit line increases the bit line parasitic capacitance.
2) Increasing cell area to integrate more memory on a single chip reduces the current that is driving the heavily loaded bit line. This causes smaller voltage swing on the bit line.
3) Decreased supply voltage lead to smaller noise margin that affects the sense amplifier reliability.[1]

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The proposed SA is shown in Fig. 1. We can observe that there are only three transistor stages cascaded from VDD to GND. Note that the transistor stage number is less than that of CLSA, and the input nodes B, Bbar are isolated to output nodes O, Obar.It is expected that the proposed SA has the same power consumption as CLSA, meanwhile a better performance at lower working voltage can be obtained.The circuit operation is described as follows.

2 CIRCUIT DIAGRAM DESCRIPTION AND OPERATION

Precharge Mode: The sensing signal SE is at logic 0. In this mode, the data on output nodes must be cleared and the SA prepares for next sensing operation. Because the sensing signals SE=0 and SEbar =1, MP1, MP4, MN5 and MN6 turn on, meanwhile MP5, MP6 turn off.Thus the input signals from bit lines can't enter through MP5 and MP6. Nodes 1 and 2 are pulled down to GND level by MN5, MN6, so MN3, MN4 will be cut off. The precharge transistors MP1, MP4 charge the output nodes to VDD. Because MN3, MN4 are turned off, both the output nodes will hold at VDD level. In this time interval, the operation detail is shown in Fig.2 (a).[2]

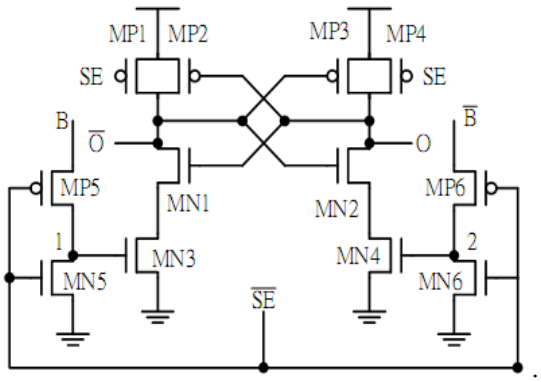

Fig.1. Proposed Sense Amplifier[2]

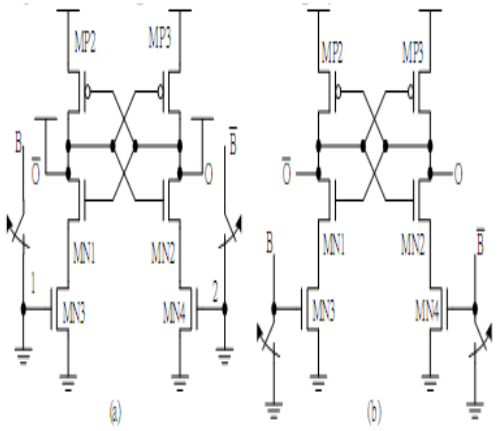

Fig.2. The proposed SA operation diagrams (a)Precharge Mode (SE=0),(b) Sense Mode (SE=1)[2]

Sense Mode: The sensing signal SE is at logic 1. In this mode, the bit line input signals B,and Bbar must be transferred to SA's differential input nodes 1 and 2. Therefore, MN3 and MN4 work as a common source differential amplifier. This operation situation is just like CLSA in sensing operation. As the sensing signals SE=1 and SEbar =0, MP5, MP6 turn on and MN5, MN6,MP1, MP4 turn off. The bit line signals are transferred to nodes 1 and 2 by MP5 and MP6.The voltage difference between nodes 1 and 2 induces a drain-to-source current difference between MN3 and MN4. Finally, the cross-coupled amplifier constructed by MP2, MP3, MN1 and MN2 will convert and amplify the current difference to a voltage difference between output nodes O, and Obar. For a very short time, the full swing logic value appears on output nodes. This operation detail is shown in Fig. 2 (b).

3 DESIGNING OF SENSE AMPLIFIER

We have completed the designing of the intended work. Our work consists of one memory cell, precharge circuitry connected with the bit lines pairs of memory. Our focus is to improve the power consumption and delay time of memory cell. Circuit diagram is shown in figure 3, which has been designed in Tanner S-edit and some parameters has been observed. Write circuitry consists of one memory cell, precharge circuitry connected with the bit lines pairs of memory shown in figure 4. For an analog designer, W/L ratio of a transistor is the main factor to achieve the desired objectives. We simulated the design for power consumption of the cell during read operation. We simulated the design and observed the power consumption which is shown in next chapter. By optimizing the value of W/L ratio of SRAM cell transistor, power consumption is improved.

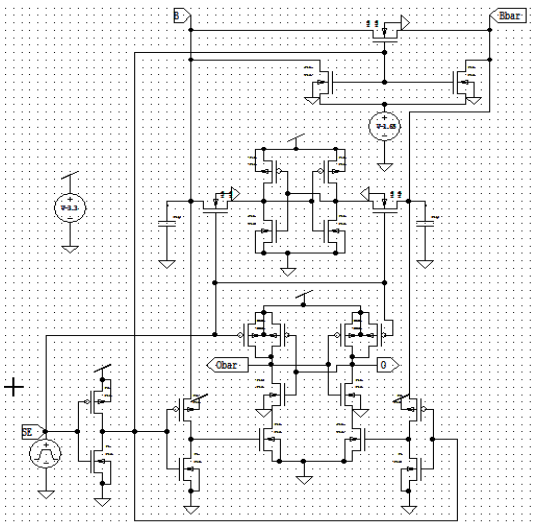

Fig.3. Designed Circuit Diagram in Tanner S-Edit Tool

4 RESULTS

We used Tanner tools- Schematic Editor (S-Edit), T-Spice and Waveform Editor (W-Edit) for simulating our design.

4.1 Read '1' Operation: In following subsection I m describing the simulation results for read '1' operation. Designed block in S-Edit is simulated and simulated waveform is described here.

4.1.1 For Output Voltage: The figure 4.1 shows the output voltage of Sense Amplifier. It is to read 1 from memory cell. Output voltage shows the logical 1 i.e. V_{dd} .. It is 0.637 ns.Sense amplifier enable signal also shown in figure.

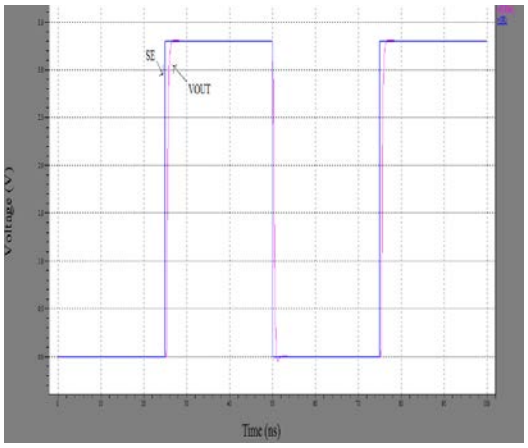

Fig.4.1. Output voltage of Sense Amplifer

4.1.2 Variation in Bitlines of Memory Cell: The figure 4.2 shows the variation in bit line voltage. Bit lines first

precharged to 1.65 V during prechage mode and when the memory cell is read, these voltage changes.

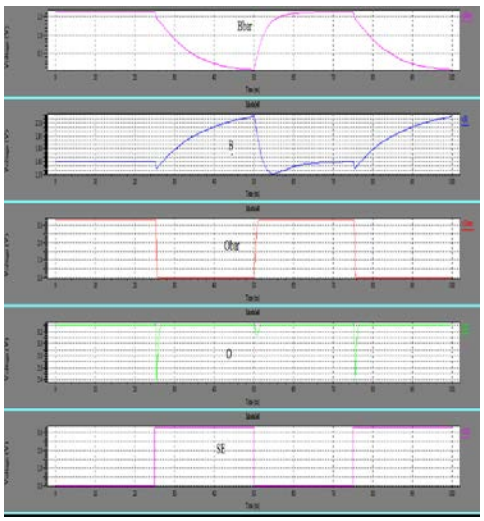

Fig. 4.2. Showing variation in bitlines voltages

4.1.3 Variation in Output Voltage of Sense Amplifier: The output of sense amplifier is complementary. One is O and another is Obar. These output voltages is shown in figure 4.3 below. Figure shows that the cell is storing 1.

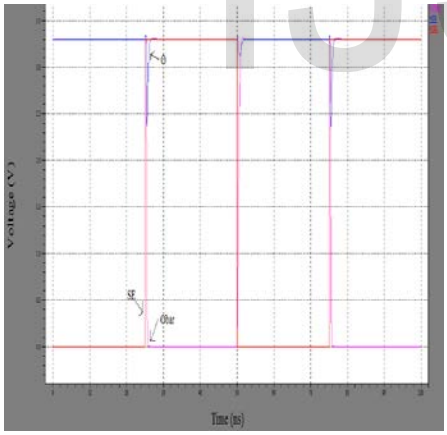

Fig.4.3: Showing variation in output nodes voltages

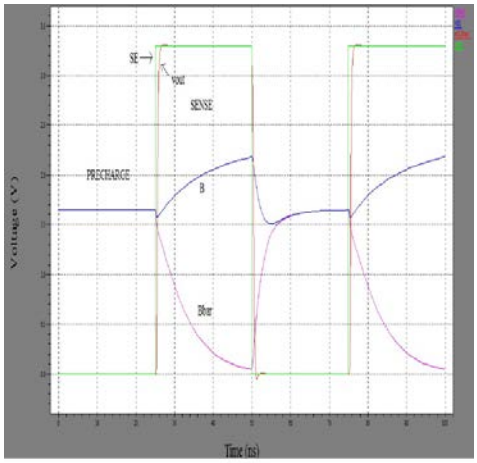

Fig.4.4 showing all signals in a single plot

4.1.4 For Power Consumption: The figure 4.5 shows power consumption during reading operation of the cell and Average power consumed is 0.206 mw.

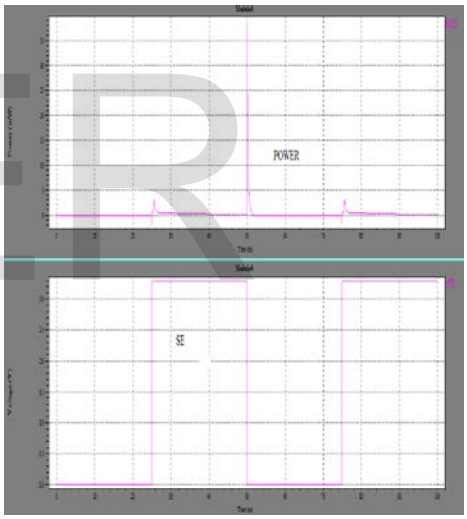

Fig. 4.5. Showing power consumption during read operation

4.2. Read '0' Operation: All simulation waveforms shown above is for reading the cell when the cell is storing '1'.Now I simulated the design for the cell which is storing '0'. I have explained the above simulation results and following results showing for memory cell when cell is storing '0'.

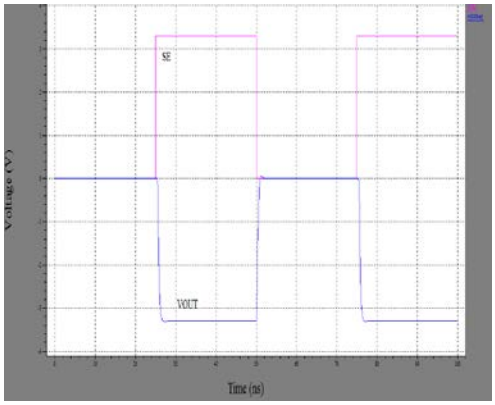

Fig. 4.6 Output voltage of sense amplifier during read 0

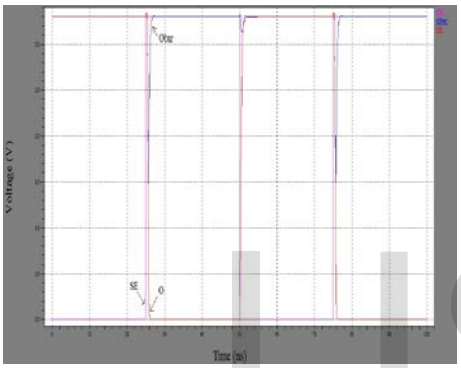

Fig.4.7 Variation in output nodes voltage during read 0

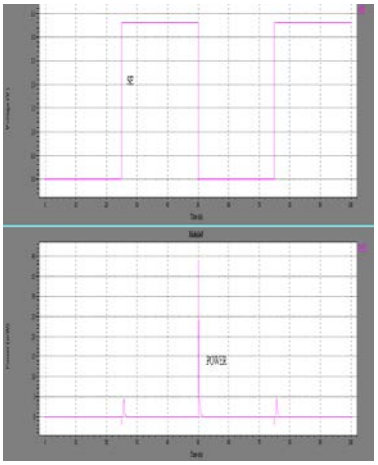

Fig.4.8. Power consumption during read 0

4.3 Simulated Results: Some important results that are observed from simulation of the schematic designed in S-Edit are summarized below.

Table 4.1: Variation in Power Consumption and Delay

S.No.	Frequency (MHz)	Power consumption(mw)	Delay (ns)
1	100	0.671	0.582
2	80	0.576	0.591
3	60	0.471	0.606
4	40	0.351	0.636
5	20	0.206	0.637
6	10	0.113	0.728

Table 4.2: Power Consumption and Delay at different load

S.No.	C_L (At 20 MHz)	Power (mw)	Delay(ns)
1	0.5	0.130	0.637
2	1	0.149	0.637
3	1.5	0.172	0.637
4	2	0.191	0.637
5	2.5	0.206	0.637
6	10	0.303	0.728

Table 4.3: Variation in Power Consumption and Delay with power supply

S.No.	Vdd (V)	Power (ms)	Delay (ns)
1	1.5	0.02	11.47
2	1.8	0.03	2.45
3	2	0.05	1.46
4	2.5	0.09	0.813
5	3	0.158	0.728
6	3.3	0.206	0.637

Table 4.4: Variation in Power Consumption and Delay with variation in transistor sizing

S.no.	Width of tail transistor of sense amplifier (um)	Power(mw)	Delay(ns)
1	1	0.204	1.46
2	2	0.207	1.09
3	4	0.207	0.819
4	8	0.206	0.637
5	16	0.208	0.546

5 CONCLUSIONS

In this work, a low power high speed Sense Amplifier design for SRAM memory is presented. The power consumption and delay factors are improved by varying the size of transistor used in Sense Amplifier..Sense amplifier is designed and simulated at 0.18µm technology. The design is implemented in CMOS technology. Power consumption and delay time of sense amplifier have been observed from simulation result. All results met specifications of the design.

6 REFERENCES

[1].Kang, Sung-Mo and Leblebici, Yusuf, "*CMOS Digital Integrated Circuits - Analysis and Design*", McGraw-Hill International Editions, Boston, 2nd Edition, 1999.

[2].Hwang-Cherng Chow, Shu-Hsien Chang,**"***High Performance Sense Amplifier Circuit for Low Power SRAM Applications***"**,ISCAS IEEE 2004, 0-7803-8251.

[3].Adel S. Sedra and Kenneth C. Smith, "*Microelectronics Circuits*" Oxford University Press International Edition, New York, 5th Edition 2006.

[4].Ardalan,S.; Chen, D.; Sachdev, M.; Kennings, A.; "*Current mode sense amplifier*" Circuits and Systems, 2005. 48th Midwest Symposium Vol. 1, 7-10 Aug. 2005 Page(s):17 – 20.Tegze P.

[5].Haraszti, Microcirc Associates "*CMOS Memory Circuits*", kluwer academic publishers New York, boston , dordrecht, London, Moscow. Pages 238-239.

[6].Chun-Lung Hsu; Mean-Horn Ho; "*High-speed sense amplifier for SRAM applications*",Volume 1, 6-9 Dec. 2004 Page(s):577 - 580 .

[7].Jan M. Rabaey, Anatha Chandrakasan and Borivoje Nikoliü, "*Digital Integrated Circuits*", Pearson Education, Inc., Second Edition, p.p. 677, 2003.

[8].Kiyoo Itoh, "*VLSI Memory Chip Design*" Springer-Verlag Berlin Heidelberg New York, p.p. 110, 2001.